This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-6.   (canceled)

7.   (currently amended):   A method for designing an integrated circuit, comprising:

        receiving data specifying a plurality of interconnects and components of a design of an integrated circuit; and

        optimizing the design of the integrated circuit, wherein data specifying the plurality of interconnects and devices of the integrated circuit is optimized based on at least one of bandwidth, latency, scalability, and isochronous interconnect configuration;

        wherein optimizing includes at least one of arranging components of the integrated circuit and specifying bandwidth between components, and

        ~~The method as described in claim 6,~~ wherein components are arranged based on latency, scalability, timing considerations, power considerations, data switching and bandwidth.

8-13.   (canceled)

14.   (previously presented):   A self-programmable integrated circuit, comprising:

        a processor suitable for performing a program of instructions, the processor accessible via a first interconnect;

        at least two components of the integrated circuit, the components communicatively connected via a second interconnect; and

        a memory suitable for storing a program of instructions;

        wherein the program of instructions configures the processor to optimize the integrated circuit based on heuristic data indicating past utilization of components of the integrated circuit,

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wherein the heuristic data includes data indicating amount of data transferred between a first component and a second component over the second interconnect, and

wherein when the data indicating the amount of data transferred over the second interconnect is less than an initially determined bandwidth, bandwidth of the second interconnect is decreased.

15. (previously presented): A self-programmable integrated circuit, comprising:

a processor suitable for performing a program of instructions, the processor accessible via a first interconnect;

at least two components of the integrated circuit, the components communicatively connected via a second interconnect; and

a memory suitable for storing a program of instructions;

wherein the program of instructions configures the processor to optimize the integrated circuit based on heuristic data indicating past utilization of components of the integrated circuit, and

wherein when the data indicating an amount of data to be transferred over the second interconnect is greater than an initially determined bandwidth, bandwidth of the second interconnect is increased.

16-23. (canceled)